



# Arm CoreLink NI-700 Non-Coherent Interconnect

## Software Developer Errata Notice

Date of issue: 04-Apr-2023

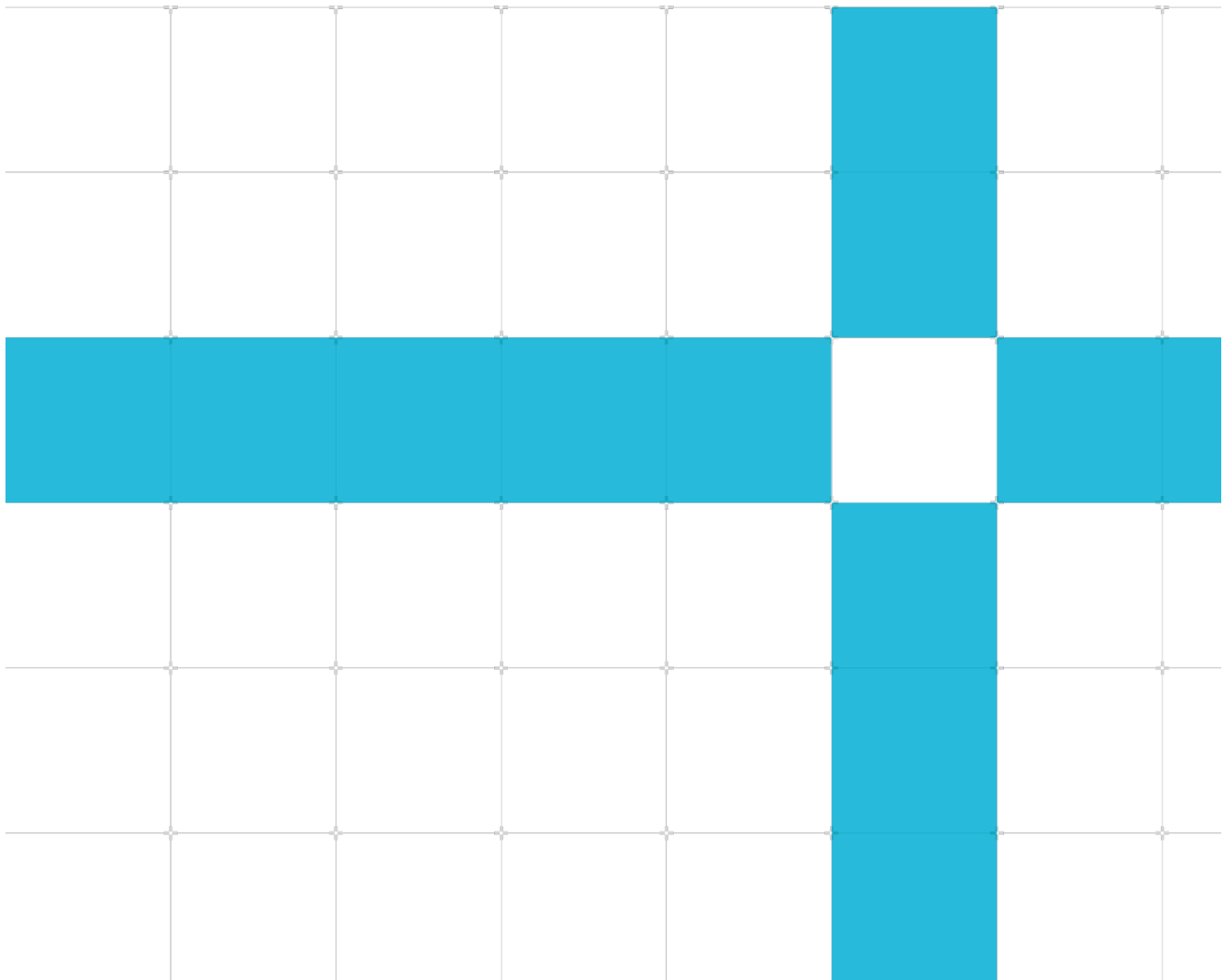
Non-Confidential

Document version: 6.0

Copyright © 2020-2023 Arm® Limited (or its affiliates). All rights reserved.

Document ID: SDEN-1780251

This document contains all known errata since the r1p0 release of the product.



## Non-confidential proprietary notice

This document is protected by copyright and other related rights and the practice or implementation of the information contained in this document may be protected by one or more patents or pending patent applications. No part of this document may be reproduced in any form by any means without the express prior written permission of Arm. No license, express or implied, by estoppel or otherwise to any intellectual property rights is granted by this document unless specifically stated.

Your access to the information in this document is conditional upon your acceptance that you will not use or permit others to use the information for the purposes of determining whether implementations infringe any third party patents.

THIS DOCUMENT IS PROVIDED "AS IS". ARM PROVIDES NO REPRESENTATIONS AND NO WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, SATISFACTORY QUALITY, NON-INFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DOCUMENT. For the avoidance of doubt, Arm makes no representation with respect to, and has undertaken no analysis to identify or understand the scope and content of, third party patents, copyrights, trade secrets, or other rights.

This document may include technical inaccuracies or typographical errors.

TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL ARM BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF ARM HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

This document consists solely of commercial items. You shall be responsible for ensuring that any use, duplication or disclosure of this document complies fully with any relevant export laws and regulations to assure that this document or any portion thereof is not exported, directly or indirectly, in violation of such export laws. Use of the word "partner" in reference to Arm's customers is not intended to create or refer to any partnership relationship with any other company. Arm may make changes to this document at any time and without notice.

If any of the provisions contained in these terms conflict with any of the provisions of any click through or signed written agreement covering this document with Arm, then the click through or signed written agreement prevails over and supersedes the conflicting provisions of these terms. This document may be translated into other languages for convenience, and you agree that if there is any conflict between the English version of this document and any translation, the terms of the English version of the Agreement shall prevail.

The Arm corporate logo and words marked with ® or ™ are registered trademarks or trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. All rights reserved. Other brands and names mentioned in this document may be the trademarks of their respective owners. Please follow Arm's trademark usage guidelines at <https://www.arm.com/company/policies/trademarks>.

Copyright © 2020-2023 Arm® Limited (or its affiliates). All rights reserved.

Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

(LES-PRE-20349)

## Confidentiality status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by Arm and the party that Arm delivered this document to.

Unrestricted Access is an Arm internal classification.

## Product status

The information in this document is for a product in development and is not final.

## Feedback

Arm welcomes feedback on this product and its documentation. To provide feedback on Arm CoreLink NI-700 Non-Coherent Interconnect, create a ticket on <https://support.developer.arm.com>.

To provide feedback on the document, fill the following survey: <https://developer.arm.com/documentation-feedback-survey>.

## Inclusive language commitment

Arm values inclusive communities. Arm recognizes that we and our industry have used language that can be offensive. Arm strives to lead the industry and create change.

If you find offensive language in this document, please email [terms@arm.com](mailto:terms@arm.com).

# Contents

<b>Introduction</b>	5
Scope	5
Categorization of errata	5
<b>Change Control</b>	6
<b>Errata summary table</b>	7
<b>Errata descriptions</b>	8
Category A	8
Category A (rare)	8
Category B	9
2247267 AHB Cacheable No-allocate transactions are converted to Non-cacheable	9
2864508 PCIe peer to peer writes blocked by atomic leading to deadlock	11
Category B (rare)	13
Category C	14
2231124 ASNI/AMNI PMU counter miscounts prefetch and write_plus_CMO transactions towards stash operations	14
2072323 HMNI SILDBG outstanding transactions field goes to 0x0 if there is a BUSY state in the middle of an AHB burst	15

# Introduction

## Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

## Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

<b>Category A</b>	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
<b>Category A (Rare)</b>	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
<b>Category B</b>	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
<b>Category B (Rare)</b>	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
<b>Category C</b>	A minor error.

# Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The [errata summary table](#) identifies errata that have been fixed in each product revision.

## 04-Apr-2023: Changes in document version v6.0

ID	Status	Area	Category	Summary
<a href="#">2864508</a>	New	Programmer	Category B	PCIe peer to peer writes blocked by atomic leads to deadlock

## 17-Sep-2021: Changes in document version v5.0

ID	Status	Area	Category	Summary
<a href="#">2247267</a>	New	Programmer	Category B	AHB Cacheable No-allocate transactions are converted to Non-cacheable
<a href="#">2231124</a>	New	Programmer	Category C	ASNI/AMNI PMU counter miscounts prefetch and writeCMO transactions towards stash operations

## 01-Apr-2021: Changes in document version v4.0

No new or updated errata in this document version.

## 15-Mar-2021: Changes in document version v3.0

ID	Status	Area	Category	Summary
<a href="#">2072323</a>	New	Programmer	Category C	HMNI SILDBG outstanding transactions field goes to 0x0 if there is a BUSY state in the middle of an AHB burst

## 30-Oct-2020: Changes in document version v2.0

No new or updated errata in this document version.

## 30-Mar-2020: Changes in document version v1.0

No errata in this document version.

# Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
<a href="#">2247267</a>	Programmer	Category B	AHB Cacheable No-allocate transactions are converted to Non-cacheable	r1p0, r2p0	r2p1
<a href="#">2864508</a>	Programmer	Category B	PCIe peer to peer writes blocked by atomic leads to deadlock	r1p0, r2p0, r2p1	Open
<a href="#">2231124</a>	Programmer	Category C	ASNI/AMNI PMU counter miscounts prefetch and writeCMO transactions towards stash operations	r1p0, r2p0	r2p1
<a href="#">2072323</a>	Programmer	Category C	HMNI SILDBG outstanding transactions field goes to 0x0 if there is a BUSY state in the middle of an AHB burst	r1p0	r2p0

# Errata descriptions

## Category A

There are no errata in this category.

## Category A (rare)

There are no errata in this category.



## Category B

2247267

### AHB Cacheable No-allocate transactions are converted to Non-cacheable

#### Status:

Fault Type: Cat-B Programmer

Fault Status: Present in r1p0, r2p0, Fixed in r2p1

#### Description:

AHB transactions presented to an HSNi as Normal Cacheable No-allocate are converted to a Normal Non-cacheable type. This can result in transactions bypassing a cache downstream of the NI-700.

#### Configurations Affected:

All the following apply:

- An HSNi has extended memory types enabled (AHB5).
- Based on the address map, the HSNi can send transactions to one or more of either:
  - An AMNI (AXI egress endpoint).
  - An HMNI that has extended memory types enabled.
- There is a cache downstream of the AMNI or HMNI.

#### Conditions:

All the following apply:

- A transaction is sent to the HSNi with HPROT[5:3] == 0b011, indicating a Normal Cacheable No-allocate transaction.
- Another observer in the system accesses the same memory locations using Normal Write-back Cacheable transactions which allocate into the cache.

In Arm Cortex-M processors with an AHB interface, Normal Cacheable No-allocate transactions are only issued if the processor includes an MPU. This includes Cortex-M23.

#### Implications:

The transaction might not look up the downstream cache. If another observer has written data into the cache that has not been written back to memory:

- An AHB read transaction might return stale data from memory.
- An AHB write transaction might leave stale data in the cache.

## Work arounds:

Software should avoid selecting a Cacheable No-allocate memory type.

- For systems with Cortex M processors, this can be done in the MPU.
- For other systems, software specific to an impacted peripheral needs to be modified to not generate Normal Cacheable No-allocate transactions.

Where a peripheral consistently emits Normal Cacheable No-allocate transactions, software may be able to treat it as a non-coherent peripheral emitting Normal Non-Cacheable transactions, provided that the Cacheable attribute upstream of the NI-700 is not visible to any other observers.

A hardware work around to the issue is to connect the HPROT[5] input to the HSN1 to what is driving the HPROT[4] input. This converts all Normal Cacheable No-allocate transactions to Normal Cacheable Allocate transactions.

## 2864508

### PCIe peer to peer writes blocked by atomic leading to deadlock

#### Status

Affects: NI-700

Fault Type: Programmer CatB

Fault Status: Present in r1p0, r2p0, r2p1. Fixed in: Open.

#### Description

This issue can happen when NI-700 is used for transport of PCIe transactions in the Root Complex, PCIe peer-to-peer traffic is present, and PCIe atomics are present.

In AMBA terms, the atomic request in question must be load/swap/compare that needs both a read and write response. Atomic requests that have both a read and a write response require an entry in both read and write trackers at the AXI subordinate (ASNI) that the request enters the NI-700 and at the AXI manager (AMNI) that the transaction exits the NI-700. Under the conditions described below, an atomic request can be blocked from making forward progress in an ASNI because it gets stuck behind a read request. Any younger write requests are blocked behind the atomic request in the ASNI's processing pipeline. Read responses are withheld in the peer PCIe controller until prior write requests have completed. Since the read responses cannot be released, there is deadlock. Note that the same behavior also applies to an AMNI.

In PCIe terms, this means a Non-Posted Read with Data (Atomic) Transaction can incorrectly block a Posted Write Transaction from making progress when Non-Posted Transaction resources are exhausted (back-pressured). If the Non-Posted Transaction resources depend on Completions ordered behind the Posted Transaction, as is the case for sustained multi-device P2P read traffic, forward progress cannot be made (deadlock).

#### Configurations Affected

This issue happens in a configuration where all the following conditions are true:

- NI-700 is used as part of the PCIe Root Complex for transport of PCIe transactions (converted to appropriate AMBA transactions)
- The PCIe Root Complex supports PCIe peer to peer transactions
- The PCIe Root Complex supports PCIe Atomic Transactions (even if only as a completer and not peer-to-peer routing)

#### Conditions

The precise conditions that cause this issue within an NI-700:

- The read channel is backpressured (stalled).

- The read channel depends on the write channel to make progress (pass the stalled reads) in order for the read backpressure to be released.
- An atomic transaction, because of this bug, causes the write channel to depend on the read channel (deadlock).

This issue is possible with the following PCIe scenario (though more complex scenarios will also expose the issue):

- Two PCIe peers are participating in traffic through the NI-700 (example sequence of transactions described below)
- Transactions issued from both PCIe controllers are:
  - PCIe peer-to-peer Non-Posted reads
  - PCIe Atomics (to any target)
  - PCIe Posted Writes (to any target)

### Sequence of Transactions

Multiple (at least two) PCIe peers must be issuing traffic that fits the following profile in order to hit the deadlock. The sequence below describes an ASNI as the block where the deadlock occurs. A similar sequence can be shown where the AMNI that supports atomic transactions is the block where the deadlock occurs.

(1) Peer to peer reads (non-posted by definition). These transactions get sent from the ASNI associated with the originating PCIe controller to the AMNI connected to its PCIe peer

(2) Peer to memory atomic

(3) Posted writes

Given transactions 1-3, the following leads to the deadlock:

(4) The PCIe controllers accept read requests from their peer (transactions (1)) until they hit the maximum number of read requests they can accept and then back pressure their AXI read request channel. This channel is being driven by the NI700 AMNI associated with that PCIe controller.

(5) The back pressure on the read request channel ripples back into the NI700 AMNI, through the NI700 interconnect, and to the ASNI connected to the peer PCIe controller that is the source of the reads.

(6) The ASNI in (5) has read requests it has accepted from its PCIe controller that can't be issued because of the backpressure

(7) The non-posted atomic (transaction (2)) is accepted by the ASNI. It incorrectly blocks the posted write transactions while for waiting for read backpressure to be removed (6).

(8) As read responses are received at the PCIe controller in (4), they are blocked because they can't bypass the write requests from (3) due to PCIe ordering rules

(9) Due to (8), the backpressure on processing read requests in the ASNI is not released and transaction (2) makes no progress, and the write transactions (3) are stuck in the ASNI behind transaction (2).

(10) Deadlock occurs because no write responses to (2) and (3) are received by the PCIe controllers, which keep them from issuing read responses.

## Implications

This leads to a deadlock

## WorkAround(s)

There is no workaround for the issue other than to avoid the conditions. For all PCIe root ports connected through the same NI-700 instance, either one of the two following options will avoid the issue:

1. Disable PCIe P2P Support through the Root Complex so that forward progress does not depend on Posted Write Transactions (or Completions) passing Non-Posted Transactions.
2. Disable PCIe Atomic Support such that the NI-700 is never presented with an Atomic Transaction on the ASNIs connected to a PCIe controller.

## Category B (rare)

There are no errata in this category.

## Category C

2231124

### ASNI/AMNI PMU counter miscounts prefetch and write\_plus\_CMO transactions towards stash operations

Status:

Fault Type: CAT C Programmer

Fault Status: Present in r1p0, r2p0. Fixed for r2p1

#### Description of Issue:

AXI slave and master network interface performance monitor event codes for cache stash operations also count AXI.H prefetch and write CMO transactions.

#### Configurations Affected:

NI-700 configurations with Prefetch\_Transaction, CMO\_On\_Write, or Write\_Plus\_CMO enabled on the ACE-Lite slave network interface.

#### Conditions:

1. AXI slave or master network interface has the PMU event select code programmed to count cache stash transactions (PMU event code = 0x13)
2. Prefetch (AWSNOOP = 0b1111), WritePtlCMO (AWSNOOP = 0b1010), WriteFullCMO (AWSNOOP = 0b1011) are received at that AXI master or slave network interface

#### Implications:

ASNI/AMNI PMU counter miscounts prefetch and write CMO transactions towards stash operations

#### WorkAround(s):

The issue only impacts the accuracy of the PMU counter itself. It has no impact on mainline functionality or performance.

Fewer AXI.H Prefetch and write CMO operations will limit the inaccuracy of the cache stash PMU count value.

## 2072323

### HMNI SILDBG outstanding transactions field goes to 0x0 if there is a BUSY state in the middle of an AHB burst

#### Status:

Fault Type: CAT-C programmer

Fault Status: Present in r1p0, Fixed in r2p0

#### Description of Issue:

During a Busy State (HTRANS = 0x1) in the middle of an AHB burst the outstanding writes, reads field currently indicates 0x0. Whereas it should continue to indicate 0x1 for the entire burst if there is an outstanding transaction.

#### Configurations Affected:

NI-700 configurations with HSNi or HMNI endpoints.

#### Conditions:

If there is a Busy State (HTRANS = 0x1) in the middle of an outstanding AHB burst.

#### Implications:

HMNI, HSNi SILDBG register does not indicate the outstanding transactions correctly.

#### WorkAround(s):

For AHB the number of outstanding transactions is not as useful when compared to AXI where there can be multiple outstanding. While there isn't a workaround for this, it is not as consequential.